ABSTRACT

An electronic package substrate for an electronic package that includes an adhesive bonding member having two planar surfaces and an orifice there through for receiving a chip and a circuitized member having two planar surfaces, one surface being bonded to one of the planar surfaces of the bonding member, said circuitized member being electrically connectable to the chip. An electronic package for a wire bonded chip or tab bonded chip that includes an adhesive bonding member having two planar surfaces and an orifice there through; a circuitized member bonded to one of the planar surfaces and having an orifice there through overlying the orifice in the bonding member; a support member bonded to the other planar surface, blocking the orifices, thereby forming a cavity; and a chip bonded within the cavity to the support member and electrically connected to the circuitized member. An electronic package substrate for an electronic package for a flip chip includes an adhesive bonding member having two planar surfaces and an orifice there through, a circuitized member bonded to one of the planar surfaces and blocking the orifice, thereby forming a cavity for receiving a flip chip, and an array of solder pads on the circuitized member within the cavity. A process for fabricating an electronic package substrate including the steps of fabricating an adhesive bonding member and a circuitized member, aligning the members with respect to each other, sandwiching the members together, and bonding the members together with heat and pressure.